REMARKS

The Office Action dated June 11, 2008, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Status of the Claims

None of the claims are amended herein. However, the claims are reproduced below for the convenience of the Examiner. Claims 1-6, 8-16 and 18 are currently pending in the application and are respectfully submitted for consideration.

Rejections under 35 U.S.C. § 103

Claims 1-6, 10, 11 and 14-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang (U.S. Patent No. 6,728,910) in view of Hidaka (U.S. Patent No. 5,933,377). The Office Action took the position on pages 3-5 that the combination of Huang and Hidaka discloses all of the features of the rejected claims. Applicant respectfully submits that Huang and Hidaka, both individually and in combination, fail to teach or suggest the features of the above-rejected claims. Reconsideration of the claims is respectfully requested.

Independent claim 1, from which claims 2-6, 8 and 9 depend, recites a method including determining if a memory section is functional based on memory BIST data, selecting a redundant memory section if the memory section is determined to be nonfunctional, and determining if at least the selected redundant memory is functional according to a BIST. The method also includes selecting a further redundant memory section if the selected redundant memory section is determined to be non-functional,

repeating selection of the further redundant memory section, if the selected further redundant memory section is non-functional, until the selected further redundant memory section is determined to be functional or all redundant memory sections have been selected, and updating a redundant memory data structure to indicate that the selected redundant memory section is no longer redundant.

Independent claim 10 recites a system including means for determining if a memory section is functional based on memory BIST data, means for selecting a redundant memory section if the memory section is determined to be nonfunctional, and means for determining if at least the selected redundant memory is functional according to a BIST. The system also includes means for selecting a further redundant memory section if the selected redundant memory section is determined to be non-functional, means for repeating selection of the further redundant memory section, if the selected further redundant memory section is non-functional, until the selected further redundant memory section is determined to be functional or all redundant memory sections have been selected, and means for updating a redundant memory data structure to indicate that the selected redundant memory section is no longer redundant.

Independent claim 11, from which claims 12-16, 18 and 19 depend, recites a system including a BIST capable of determining if a memory section is functional and self-adaptive logic, communicatively coupled to the BIST, capable of selecting a redundant memory section if the memory section is determined to be nonfunctional. The BIST is further capable of determining if at least the selected redundant memory is

functional, and selecting a further redundant memory section if the selected redundant memory section is determined to be non-functional. The BIST is also capable of repeating selection of the further redundant memory section, if the selected further redundant memory section is non-functional, until the selected further redundant memory section is determined to be functional or all redundant memory sections have been selected, and updating a redundant memory data structure to indicate that the selected redundant memory section is no longer redundant.

As will be discussed below, Huang and Hidaka, both individually and in combination, fail to disclose or suggest the features of the presently pending claims.

Huang generally discusses "test and repair of semiconductor memory" (column 1, lines 8 and 9). "Rather than relying on separate BIST mechanisms to test the redumdant and accessible memory arrays, a single generic BIST may be used to simultaneously test acceptable and redundant portions of the memory" (column 3, lines 27-31, of Huang). "The method disclosed herein may be used for self-test and self-repair of a memory comprising first and second arrays" (column 3, lines 37 and 38, of Huang). "The first array represents the accessible portion of the memory and the second array the redundant portion" (column 3, lines 49 and 50, of Huang). "The repair operation consists of recording the addresses of failing accessible rows in a repair table; associated with each of these addresses is the address of a non-failing redundant row. Using the repair table, the BISR dynamically substitutes a good redundant row for every failing accessible row" (column 3, lines 53-58, of Huang).

Hidaka generally discusses "a redundant structure for defect repair in a semiconductor memory device and a structure for simplifying a test therefor" (column 1, lines 10-12). "[A] semiconductor memory device comprises a memory cell array having a plurality of dynamic memory cells, and memory cell access means accessing the plurality of memory cells on the basis of address signals respectively in a refresh operation" (column 2, lines 17-22, of Hidaka). "[T]he memory cell access means is accessible to the plurality of memory cells at a plurality of refresh intervals in the refresh operation" (column 2, lines 22-24, of Hidaka).

Independent claim 1 recites, in part, "selecting a further redundant memory section if the selected redundant memory section is determined to be non-functional" and "repeating selection of the further redundant memory section if the selected further redundant memory section is non-functional, until the selected further redundant memory section is determined to be functional or all redundant memory sections have been selected". Independent claims 10 and 11, which each have their own scope, recite similar features. The Office Action admitted on page 2 that Huang fails to teach these features, but rather asserted on page 3 that column 4, lines 14-33 of Hidaka cure these deficiencies of Huang. Applicant respectfully disagrees.

The cited section of Hidaka discusses:

> (a) testing whether or not the defective block is present in the plurality of normal cell array blocks;
> (b) carrying out a defectiveness/non-defectiveness test on at least one spare cell array block when presence of the defective block is confirmed in the test at the step (a); and

(c) making change for accessing one block among at least one spare cell array block in place of the defective block and carrying out defect repair when a determination of non-defectiveness is made in the defectiveness/non-defectiveness test at the step (b).

(Column 4, lines 16-25, of Hidaka). Thus, if a defective block is confirmed, Hidaka carries out a defectiveness/non-defectiveness test on at least one spare cell array block. However, claim 1 recites selecting a **further** redundant memory section if the selected redundant memory section is non-functional. Selection of a further redundant memory section is repeated if said section is determined to be non-functional, and this process is repeated until: 1) a functional block is found, or 2) all of the redundant memory sections have been selected. In other words, the selection process applied in claim 1 is **iterative**. On the other hand, Hidaka merely discusses that at least one spare cell array block is tested, without disclosing, teaching or suggesting any such iterative process. Also, it does not appear that the cited section of Hidaka takes into account a case where all of the redundant memory sections are defective.

One advantage of this iterative testing method in some embodiments is that iteratively testing redundant memory sections only until a functional section is found is that once such a section is found, no additional processing is required. While Hidaka discusses that a defectiveness test may be performed on at least one spare cell array block, testing multiple blocks would waste processing resources if more than one block is functional. Accordingly, certain embodiments of the present invention are able to achieve higher processing efficiency than is possible with Hidaka.

Independent claim 1 also recites, in part, "updating a redundant memory data structure to indicate that the selected redundant memory section is no longer redundant." Independent claims 10 and 11, which each have their own scope, recite similar features. The Office Action took the position on page 2 that Huang teaches these features. Applicant respectfully disagrees.

The Office Action stated on page 2 that "Huang discloses updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant in column 3, lines 53-58. The redundant memory section is no longer redundant when it is used to replace a faulty row." The cited section of Huang discusses that "[t]he repair operation consists of recording the addresses of failing accessible rows in a repair table; associated with each of these addresses is the address of a non-failing redundant row. Using the repair table, the BISR dynamically substitutes a good redundant row for every failing accessible row." Thus, addresses of failed rows are recorded in a repair table, and addresses of non-failing redundant rows are associated with the failed rows.

However, the cited section of Huang does not teach updating a redundant memory data structure to indicate that the selected redundant memory section **is no longer redundant**. Rather, it appears that Huang merely uses a repair table to indicate failing rows and associate non-failing redundant rows therewith. There is no disclosure, teaching or suggestion that Huang actually updates a redundant memory data structure (such as the second array discussed in Huang) to indicate that certain sections of memory

are no longer redundant. Further, nothing is cited or found in Hidaka that overcomes these deficiencies of Huang.

Claim 3 recites "outputting a pass or fail signal based on the determining if at least the selected redundant memory is functional according to a BIST." Independent claim 13, which has its own scope, recites similar features. The Office Action stated on page 3 that these features are disclosed by column 9, lines 10-13, of Huang, without providing reasoning. Applicant respectfully disagrees.

The cited section of Huang discusses that "[i]f an error occurs in the first m rows during the second stage, the memory is considered non-repairable, and the BISR toggles the externally accessible FAIL flag 84." However, on the other hand, claim 3 recites outputting a **pass** or fail signal - in other words, one or the other. Huang does not appear to be capable of outputting a "pass" signal. Rather, as can be seen in Fig. 5, the three flags output from the BISR are ERRN, FAIL and DONE - none of which correspond with a "pass" signal.

Further, Applicant respectfully submits that the Office Action did not make a *prima facie* case of obviousness with respect to the above-rejected claims. For the most part, it appears that the Office Action "cut-and-pasted" the claim recitations and appended citations to Huang and/or Hidaka thereto. For example, the Office Action stated on page 3, after copying certain features of claim 1, that "Hidaka discloses this limitation in column 4, lines 14-33." However, no support for this conclusory assertion is

provided on the record. Applicant respectfully submits that in order to make a *prima facie* case of obviousness, reasoning must be provided for the rejection of each feature.

MPEP § 2143 states that "[t]he key to supporting any rejection under 35 U.S.C. 103 is the **clear articulation** of the reason(s) why the claimed invention would have been obvious. The Supreme Court in *KSR* noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made **explicit**" (emphasis added). Because the rejection lacks a clear articulation of the reasons why the rejected features would allegedly have been obvious in view of Huang and Hidaka, the rejection cannot be supported per the requirements set forth by the United States Supreme Court. Without such reasoning, there is no indication on the record for a court or any other subsequent reader of the file wrapper as to **why** the features of the claims were believed to have been taught by the cited art. Applicant respectfully notes that at least because the Office Action failed to establish a *prima facie* case of obviousness, any rejection in a subsequent Office Action providing adequate reasoning would be presented for the first time on the record and as such, a next Action **cannot** be made final.

Claims 2-6 and 14-16 depend from claims 1 or 11 and add further features thereto. Thus, the arguments above with respect to the independent claims also apply to the dependent claims.

Per the above, Huang and Hidaka, both individually and in combination, fail to teach or suggest all of the features of the above-rejected claims. Accordingly, it is

respectfully submitted that the rejection is overcome and respectfully requested that the rejection be withdrawn.

Claim 12 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang in view of Hidaka and further in view of Huang (U.S. Publication No. 2002/0136066, hereinafter "Huang Pub"). Claim 12 depends from independent claim 11 and adds further features thereto. Nothing is cited or found in Huang Pub, which generally discusses "test and repair of semiconductor memory" (paragraph [0002]), that overcomes the deficiencies of Huang and Hidaka discussed above with respect to the independent claims. Thus, the arguments above with respect to the independent claims also apply to claim 12.

Accordingly, it is respectfully submitted that the rejection is overcome and respectfully requested that the rejection be withdrawn.

Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang in view of Hidaka and further in view of Tanizaki et al. (U.S. Patent No. 6,993,696). Claim 13 depends from independent claim 11 and adds further features thereto. Nothing is cited or found in Tanizaki et al., which generally discusses "a semiconductor memory device with a built-in self test circuit" (column 1, lines 9 and 10), that overcomes the deficiencies of Huang and Hidaka discussed above with respect to the independent claims. Thus, the arguments above with respect to the independent claims also apply to claim 13.

Accordingly, it is respectfully submitted that the rejection is overcome and respectfully requested that the rejection be withdrawn.

Claims 8 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang in view of Hidaka and further in view of Aipperspach et al. (U.S. Patent No. 6,181,614). Claims 8 and 18 depends from independent claims 1 or 11 and add further features thereto. Nothing is cited or found in Aipperspach et al., which generally discusses "the repair of faulty memory cells in solid state memory arrays" (column 1, lines 6 and 7), that overcomes the deficiencies of Huang and Hidaka discussed above with respect to the independent claims. Thus, the arguments above with respect to the independent claims also apply to claims 8 and 18.

Accordingly, it is respectfully submitted that the rejection is overcome and respectfully requested that the rejection be withdrawn.

Claims 9 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang in view of Hidaka and further in view of Cheston et al. (U.S. Publication No. 2003/0014619). Claims 9 and 19 depends from independent claims 1 or 11 and add further features thereto. Nothing is cited or found in Cheston et al., which generally discusses "setting up and executing a protected copy of a master boot record such that upon a booting failure, the system can be recovered without the need for an external bootable media" (paragraph [0002]), that overcomes the deficiencies of Huang and Hidaka discussed above with respect to the independent claims. Thus, the arguments above with respect to the independent claims also apply to claims 9 and 19.

Accordingly, it is respectfully submitted that the rejection is overcome and respectfully requested that the rejection be withdrawn.

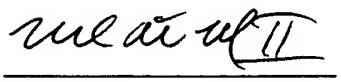
Conclusion

For at least the reasons presented above, it is respectfully submitted that claims 1-6, 8-16 and 18, comprising all of the currently pending claims, patentably distinguish over the cited art. Accordingly, it is respectfully requested that the claims be allowed and the application be passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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